Although not specifically clear from the Office Action, it appears that the Examiner is suggesting that all of the memories **202** of all of the controllers **104** in the Hubis '298 patent together collectively constitute a shared memory that allows for concurrent access via their individual connections **140** to the host and that the bus **110** is a copy bus to each memory **202**. Applicant disagrees with this characterization of the prior art.

As an initial point amended independent Claim 1 recites that at least two ports for each memory have a concurrent-access function. This means that at least two of the ports for each memory can be used concurrently to gain access to the memory. Further, amended independent Claim 1 recites that at least one of these ports further has a copy-bus function, while the other port can be accessed from a user side. What this means is that information can be copied to the memory via the copy-bus port while at the same time, (i.e., concurrently), information is accessed from the memory via the other port from the user side. Dependent Claim 6 was added to demonstrate additionally that in some embodiments each memory could have a plurality of ports all having a concurrent-access function, such that multiple concurrent accesses to the memory can be made.

As a first point, the memories **202** of each controller **104** of the Hubis '298 patent pointed to by the previous Office Action as constituting the "shared memory" are in fact, not a shared memory at all. Specifically, a shared memory is defined in the art as a memory capable of supplying an identical database to several users, i.e., sharing the possibility of read and write accesses to identical data by all users. The memories **202** for each controller **104** of the Hubis '298 patent, on the other hand, do not supply identical databases for several users. Instead, each of these memories **202** only includes data that has been altered during processing and does not contain an entire record of all data. Specifically, as data is written to the shared storage devices **108** during processing, this written data is also stored in the memories **202** for each controller **104**. Any data located in shared memory **108** that is only read and not altered is not also stored in the memories **202** of each controller. As such, the memories **202** of each controller **104** only include data that has been written into the shared memory, but does not include all of the data stored in the shared memory **108**. As such, each of the memories **202** of the controllers **104** does

not provide an identical database to all users and therefore cannot be characterized as shared memories.

Instead, the Hubis '298 patent requires the memories **202** of each controller **104** in combination with the memory devices **108** to create a shared memory. Because, the memories **202** for each controller **104** do not include a complete copy of all data and thus are not a shared memory, the controllers themselves cannot be seen as meeting the plurality of memories as recited in amended independent Claim 1. For the Hubis '298 patent to arguably meet the claimed invention, each controller **104** in combination with the shared memory **108** must be compared to amended independent Claim 1. In this instance, the system of the Hubis '298 patent further does not teach or suggest the claimed invention.

The combination of each controller **104** with the shared memory **108** does not provide at least two ports that allow for internally concurrent accesses to the memories as recited in amended independent Claim 1. The memory **108** is connected via the bus **110** to each of the controllers **104**. Because there is only one access bus **110** connected between the controllers **104** and the memory **108**, there cannot be concurrent accesses to the memory in the Hubis '298 patent. In the Hubis '298 patent, if the host computer **102** requests data from a controller **104** that is not located in the controller's memory **202**, the controller must access the memory **108** via the bus **110**. This action blocks all of the other controllers **104** from using the bus **110**. As such, concurrent access of the shared memory, as recited in amended independent Claim 1, is not possible using the system of the Hubis '298 patent.

As mentioned previously and reiterated here, the combination of the Gujral '260 and Hamaguchi '472 patents with the Hubis '296 patent does not teach or suggest a shared memory having true multi-port memories. Specifically, the Gujral '260 and Hamaguchi '472 patents do not disclose true multi-port memories. Instead, they disclose only pseudo two-port memories. They include controllers, (which a true two-port memory would not have), to turn concurrent accesses from the two ports into sequential accesses. As such, their pseudo two-port memories support only one concurrent access to two ports, while the true multi-port memory of the claimed invention supports N concurrent accesses to N ports.

In light of the above, Applicant respectfully submits that none of the cited references, taken either individually or in combination, teaches or suggests a shared memory having true multi-port memories as recited in amended independent Claim 1. As such, Applicant respectfully submits that amended independent Claim 1, as well as the claims that depend therefrom, is patentable over the cited references.

CONCLUSION

In view of the amended claims and the remarks presented above, it is respectively submitted that all of the present claims of the application are in condition for immediate allowance. It is therefore respectfully requested that a Notice of Allowance be issued. The Examiner is encouraged to contact Applicant's undersigned attorney to resolve any remaining issues in order to expedite examination of the present application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of

this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,

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"Express Mail" Mailing Label Number EV 034185431 US Date of Deposit: November 12, 2002 I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box Patent Application, Commissioner for Patents, Washington, DC 20231. _____	**CERTIFICATE OF MAILING** I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on November 20, 2002. Elaine Kelly Elaine Kelly

Version With Markings to Show Changes Made:

In the Claims:

Please amend Claim 1 as follows:

1. (Thrice Amended) A shared memory comprising:

a plurality of [true] multi-port memories, wherein each memory has at least two [access] ports, wherein each port has a concurrent-access function that allows [accessible from a user side, wherein said at least two access ports allow] for internally concurrent access via the port to data stored in the memory, wherein at least one of said at least two ports has [each memory further has at least one port with] a copybus-function and wherein at least one of said at least two ports is accessible from a user side [separate from said at least two access ports]; and

at least one copybus connected to each of said at least one ports having the copybus-function;

wherein said shared memory is adapted to copy contents of one of said multi-port memories, which has been changed by a writing operation from said user side, to other multi-port memories through said at least one copybus.